------------------MAIN CODE----------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating

---- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity Code is

Port ( a : in STD\_LOGIC\_VECTOR (3 downto 0);

b : in STD\_LOGIC\_VECTOR (03 downto 0);

s : in STD\_LOGIC\_VECTOR (02 downto 0);

y : out STD\_LOGIC\_VECTOR (03 downto 0));

end Code;

architecture Behavioral of Code is

begin

with s select

y <= a+b when "000",

a-b when "001",

a and b when "010",

a or b when "011",

a nand b when "100",

a nor b when "101",

a xor b when "110",

a when others;

end Behavioral;

--------------TEST BENCH CODE------------

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

USE ieee.std\_logic\_unsigned.all;

USE ieee.numeric\_std.ALL;

ENTITY test1\_vhd IS

END test1\_vhd;

ARCHITECTURE behavior OF test1\_vhd IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT Code

PORT(

a : IN std\_logic\_vector(3 downto 0);

b : IN std\_logic\_vector(3 downto 0);

s : IN std\_logic\_vector(2 downto 0);

y : OUT std\_logic\_vector(3 downto 0)

);

END COMPONENT;

--Inputs

SIGNAL a : std\_logic\_vector(3 downto 0) := (others=>'0');

SIGNAL b : std\_logic\_vector(3 downto 0) := (others=>'0');

SIGNAL s : std\_logic\_vector(2 downto 0) := (others=>'0');

--Outputs

SIGNAL y : std\_logic\_vector(3 downto 0);

BEGIN

-- Instantiate the Unit Under Test (UUT)

uut: Code PORT MAP(

a => a,

b => b,

s => s,

y => y

);

tb : PROCESS

BEGIN

-- Wait 100 ns for global reset to finish

wait for 100 ns;

a<= "1010";

b<="1000";

s<="000";

wait for 50 ns;

s<="001";

wait for 50 ns;

s<="010";

wait for 50 ns;

s<="011";

wait for 50 ns;

s<="100";

wait for 50 ns;

s<="101";

wait for 50 ns;

s<="110";

wait for 50 ns;

s<="111";

wait for 50 ns;

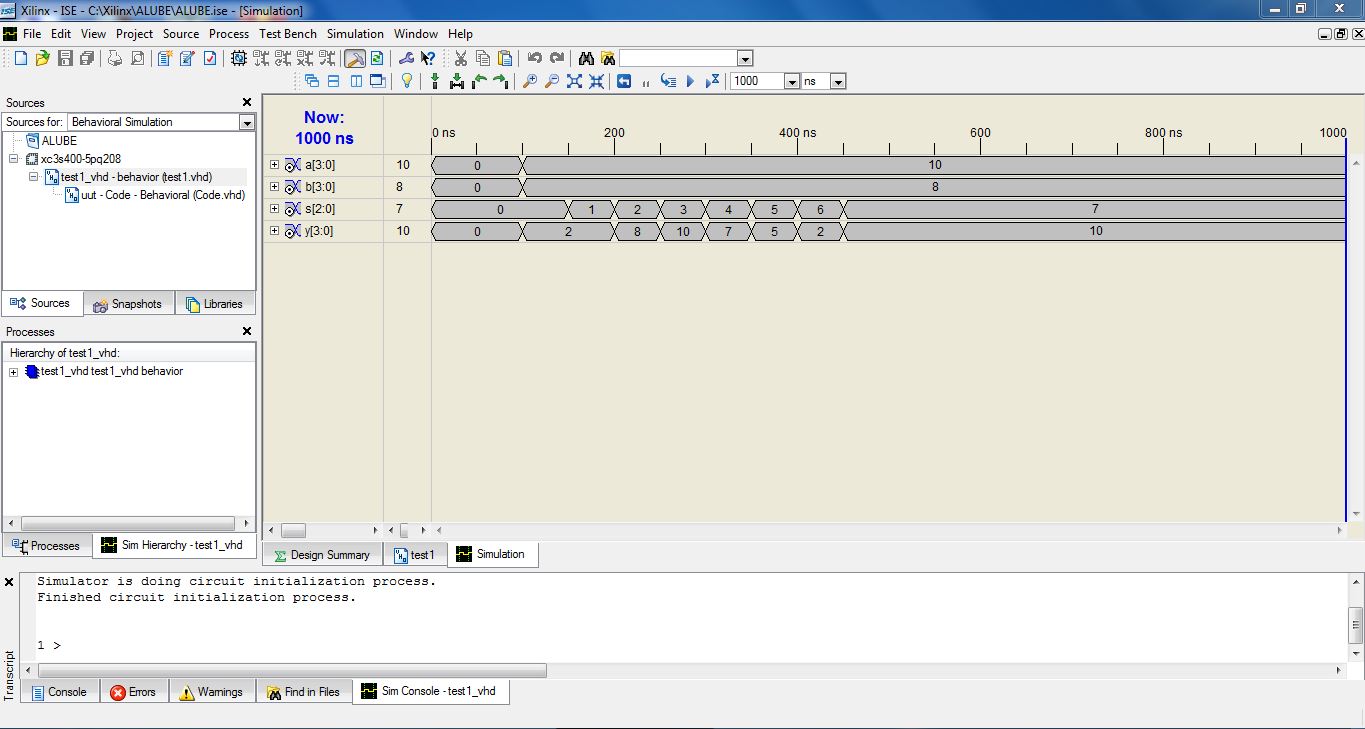
-- Place stimulus here

wait; -- will wait forever

END PROCESS;

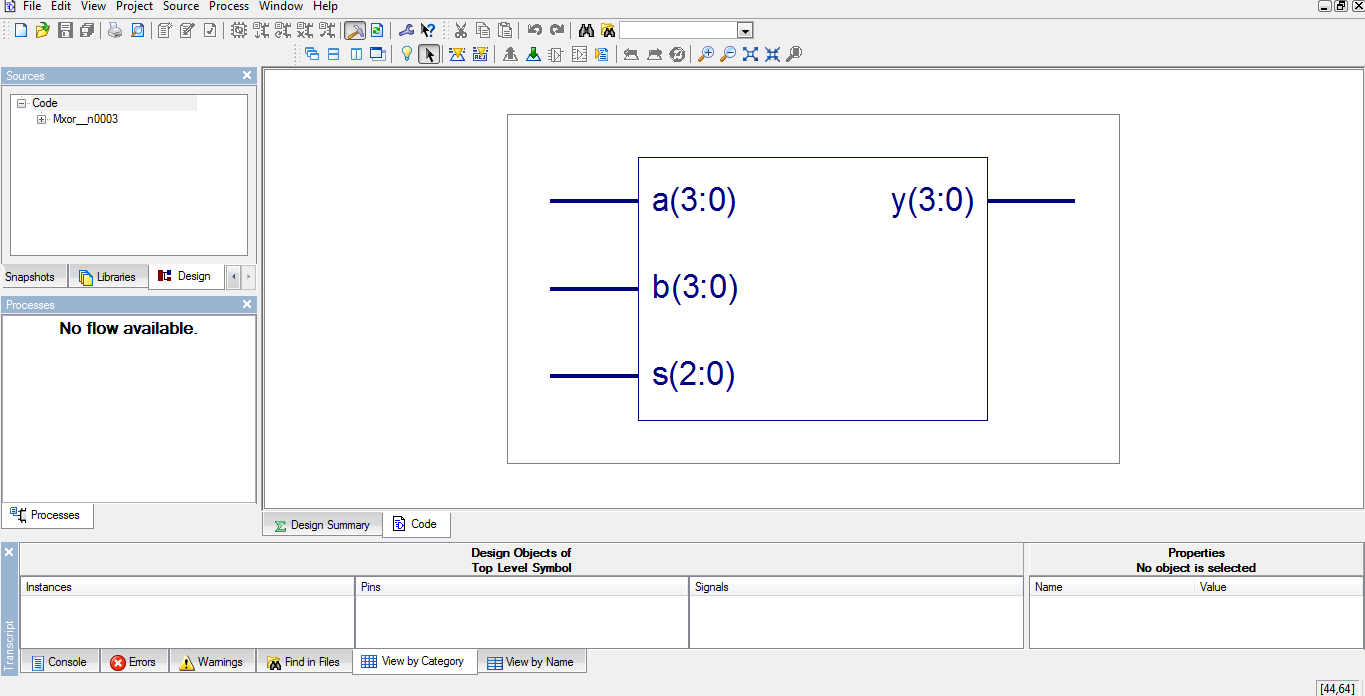
END;

----------TESHBENCH WAVEFORM--------------

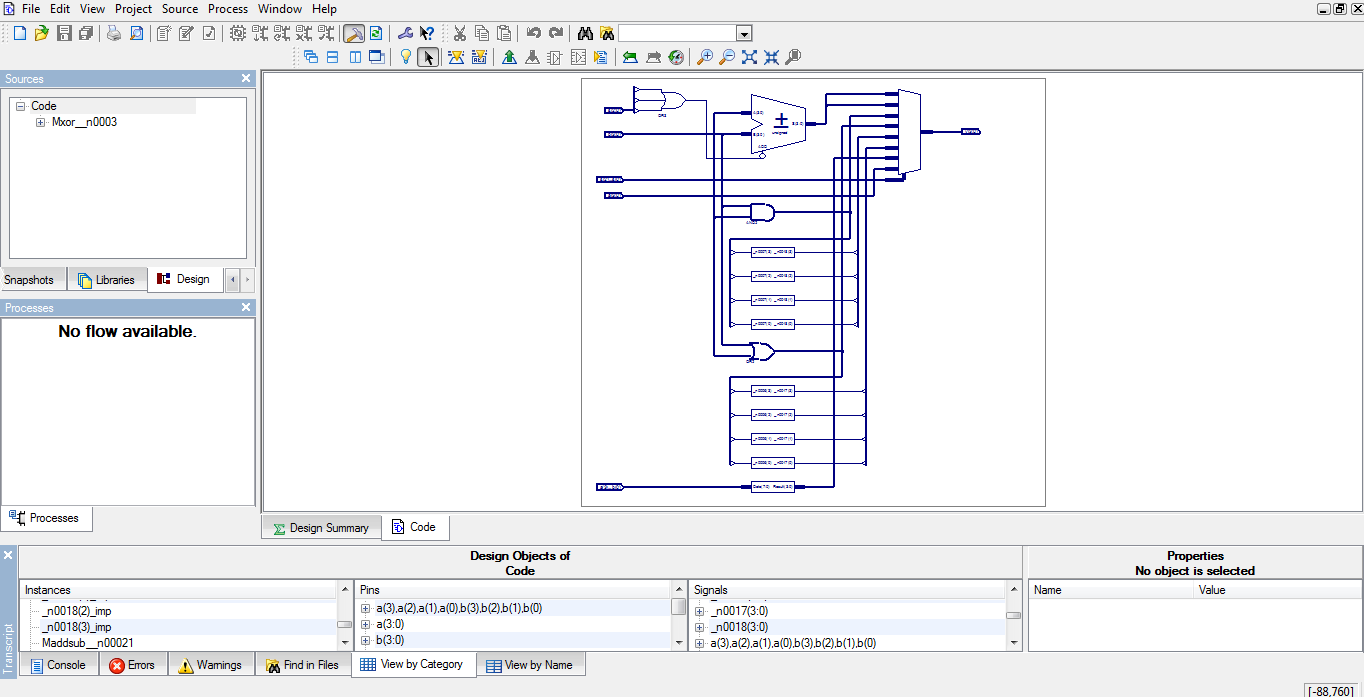


-------------RTL SCHEMATIC-------------------

1.



2.



------------PINASSIGNEMNT-----------------

